CLAIMS

1. A semiconductor device comprising;

a semiconductor substrate; and

a multi-layered wiring arrangement provided on said semiconductor substrate, said multi-layered wring arrangement including at least one insulating layer structure having a metal wiring constitution formed therein,

wherein said insulating layer structure includes a first SiOCH layer, a second SiOCH layer formed on said first SiOCH layer, and a silicon dioxide (SiO_2) layer formed on said second SiOCH layer, and said second SiOCH layer features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer.

2. A semiconductor device as set forth in claim 1, wherein said first SiOCH layer features the carbon (C) density falling in a range between 10 atoms % and 20 atoms %, the oxygen (O) density falling in a range between 20 atoms % and 35 atoms %, and the hydrogen (H) density of more than 25 atoms %, and said second SiOCH layer features the carbon (C) density of less than 10 atoms %, the oxygen (O) density of more than 35 atoms %, and the hydrogen (H) density of less than 25 atoms %.

3. A semiconductor device as set forth in claim 1, wherein said insulating layer structure has a trench pattern formed therein, and said metal wiring constitution comprises a metal wiring pattern buried in said trench pattern.

4. A semiconductor device as set forth in claim 3, wherein said metal wiring pattern is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said trench pattern to thereby prevent diffusion of copper atoms from said copper wiring pattern into said insulating layer

structure.

5. A semiconductor device as set forth in claim 4, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

6. A semiconductor device as set forth in claim 5, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

7. A semiconductor device as set forth in claim 4, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

8. A semiconductor device as set forth in claim 7, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

9. A semiconductor device as set forth in claim 4, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

10. A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

11. A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered

structure comprising a SiCNH layer and a SiCH layer.

12. A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

13. A semiconductor device as set forth in claim 9, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

14. A semiconductor device as set forth in claim 4, wherein said copper wiring pattern contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

15. A semiconductor device as set forth in claim 1, wherein said insulating layer structure has at least one hole formed therein, and said metal wiring constitution comprises a metal via-plug buried in said hole.

16. A semiconductor device as set forth in claim 15, wherein said metal via-plug is made of copper (Cu), and a barrier metal layer is formed on wall faces defining said hole to thereby prevent diffusion of copper atoms from said copper via-plug into said insulating layer structure.

17. A semiconductor device as set forth in claim 16, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

18. A semiconductor device as set forth in claim 17, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum

compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

19. A semiconductor device as set forth in claim 16, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

20. A semiconductor device as set forth in claim 19, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

21. A semiconductor device as set forth in claim 16, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

22. A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

23. A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

24. A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

25. A semiconductor device as set forth in claim 21, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

26. A semiconductor device as set forth in claim 16, wherein said copper via-plug contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

27. A semiconductor device as set forth in claim 1, wherein said insulating layer structure has a trench pattern formed therein, and at least one hole formed in a bottom of said trench pattern, and said metal wiring constitution comprises a metal wiring pattern buried in said trench pattern, and a metal via-plug buried in said hole.

28. A semiconductor device as set forth in claim 27, wherein said metal wiring pattern and said metal via-plug are made of copper (Cu), and a barrier metal layer is formed on wall faces defining both said trench pattern and said hole to thereby prevent diffusion of copper atoms from said copper wiring pattern and said copper via-plug into said insulating layer structure.

29. A semiconductor device as set forth in claim 28, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

30. A semiconductor device as set forth in claim 29, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

31. A semiconductor device as set forth in claim 28, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group

consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

32. A semiconductor device as set forth in claim 31, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

33. A semiconductor device as set forth in claim 28, wherein said insulating layer structure further includes a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

34. A semiconductor device as set forth in claim 33, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

35. A semiconductor device as set forth in claim 33, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

36. A semiconductor device as set forth in claim 33, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

37. A semiconductor device as set forth in claim 33, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

38. A semiconductor device as set forth in claim 28, wherein said copper wiring pattern contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au),

mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

39. A method of manufacturing a semiconductor device comprising:

preparing a semiconductor substrate on which a multi-layered wiring arrangement be provided; and

forming at least one insulating layer structure, having a metal wiring constitution, to thereby construct said multi-layered wiring arrangement,

wherein the formation of said insulating layer structure comprises:

producing a first SiOCH layer;

treating a surface section of said first SiOCH layer such that the surface section of said first SiOCH layer is produced and defined as a second SiOCH layer which features a carbon (C) density lower than that of said first SiOCH layer, a hydrogen (H) density lower than that of said first SiOCH layer, and an oxygen (O) density higher than that of said first SiOCH layer;

forming a silicon dioxide (SiO_2) layer formed on said second SiOCH layer; and

forming said metal wiring constitution in said first and second SiOCH layers and said silicon dioxide (SiO_2) layer.

40. A method as set forth in claim 39, wherein said first SiOCH layer features the carbon (C) density falling in a range between 10 atoms % and 20 atoms %, the oxygen (O) density falling in a range between 20 atoms % and 35 atoms %, and the hydrogen (H) density of more than 25 atoms %, and said second SiOCH layer features the carbon (C) density of less than 10 atoms %, the oxygen (O) density of more than 35 atoms %, and the hydrogen (H) density of less than 25 atoms %.

41. A method as set forth in claim 39, wherein the treatment of the surface section of said first SiOCH layer is

carried out by reforming and modifying said surface section with a plasma treatment using a first gas from which oxygen (O), hydrogen (H), and nitrogen (N) are excluded, and with a thermal oxidization treatment using a second gas including oxygen (O).

42. A method as set forth in claim 41, wherein said first gas comprises a helium (He) gas.

43. A method as set forth in claim 41, wherein said first gas comprises an inert gas.

44. A method as set forth in claim 43, wherein said inert gas is an argon (Ar) gas.

45. A method as set forth in claim 41, wherein said second gas comprises at least one selected from a group consisting of an oxygen (O_2) gas, an ozone (O_3) gas, a nitrous oxide (N_2O) gas, an nitrogen monoxide (NO) gas, a carbon monoxide (CO) gas, and a carbon dioxide (CO_2) gas.

46. A method as set forth in claim 39, wherein both the treatment of the surface section of said first SiOCH layer and the formation of said silicon dioxide (SiO_2) layer are carried out in a closed vessel defining a processing chamber without said first SiOCH layer's being exposed to atmosphere.

47. A method as set forth in claim 39, wherein the formation of said metal wiring constitution is carried out by:

forming a trench pattern in said first and second SiOCH layers and said silicon dioxide (SiO_2) layer; and

forming a metal wiring pattern by filling said trench pattern with a metal material.

48. A method as set forth in claim 47, wherein said metal material is copper (Cu), and a barrier metal layer is formed on wall faces defining said trench pattern to thereby prevent diffusion of copper atoms from said copper wiring pattern into said first and second SiOCH layers and said silicon dioxide (SiO_2) layer, before said trench pattern is filled with the

copper (Cu).

49. A method as set forth in claim 48, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

50. A method as set forth in claim 49, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

51. A method as set forth in claim 48, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

52. A method as set forth in claim 51, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

53. A method as set forth in claim 48, wherein the formation of said insulating layer structure further comprises forming a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

54. A method as set forth in claim 53, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

55. A method as set forth in claim 53, wherein said barrier insulating layer has a multi-layered structure

comprising a SiCNH layer and a SiCH layer.

56. A method as set forth in claim 53, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

57. A method as set forth in claim 53, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

58. A method as set forth in claim 48, wherein said copper wiring pattern contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

59. A method as set forth in claim 39, wherein the formation of said metal wiring constitution is carried out by:

forming at least one hole in said first and second SiOCH layers and said silicon dioxide (SiO_2) layer; and

forming a metal via-plug by filling said hole with a metal material.

60. A method as set forth in claim 59, wherein said metal material is copper (Cu), and a barrier metal layer is formed on wall faces defining said hole to thereby prevent diffusion of copper atoms from said copper via-plug into said first and second SiOCH layers and said silicon dioxide (SiO_2) layer, before said hole is filled with the copper (Cu).

61. A method as set forth in claim 60, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

62. A method as set forth in claim 61, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is

either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

63. A method as set forth in claim 60, wherein said barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

64. A method as set forth in claim 63, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

65. A method as set forth in claim 60, wherein the formation of said insulating layer structure further comprises forming a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

66. A method as set forth in claim 65, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

67. A method as set forth in claim 65, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

68. A method as set forth in claim 65, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

69. A method as set forth in claim 65, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

70. A method as set forth in claim 60, wherein said copper

via-plug contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn), lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).

71. A method as set forth in claim 39, wherein the formation of said metal wiring constitution is carried out by:

forming a trench pattern in said first and second SiOCH layers and said silicon dioxide (SiO_2) layer;

forming at least one hole formed in a bottom of said trench pattern; and

forming a metal wiring pattern with at least metal via-plug by filling both said trench pattern and said hole with a metal material.

72. A method as set forth in claim 71, wherein said metal material is copper (Cu), and a metal barrier layer is formed on wall faces defining both said trench pattern and said hole to thereby prevent diffusion of copper atoms from said copper wiring pattern and said copper via-plug into said first and second SiOCH layers and said silicon dioxide (SiO_2) layer, before said trench pattern and said hole is filled with the copper (Cu).

73. A method as set forth in claim 72, wherein said barrier metal layer has a single-layered structure, which is formed of one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

74. A method as set forth in claim 73, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

75. A method as set forth in claim 72, wherein said

barrier metal layer has a multi-layered structure, which is formed of more than one selected from a group consisting of titanium (Ti), a titanium compound, tantalum (Ta), and a tantalum compound.

76. A method as set forth in claim 75, wherein said titanium compound is either titanium nitride (TiN) or titanium silicon nitride (TiSiN), and said tantalum compound (Ta) is either tantalum nitride (TaN) or tantalum silicon nitride (TaSiN).

77. A method as set forth in claim 72, wherein the formation of said insulating layer structure further comprises forming a barrier insulating layer on which said first SiOCH layer is formed, and said barrier insulating layer prevents diffusion of copper atoms into said first SiOCH layer when said insulating layer structure is formed on another insulating layer structure having a copper wiring constitution.

78. A method as set forth in claim 77, wherein said barrier insulating layer has a single-layered structure comprising either a SiCNH layer or a SiCH layer.

79. A method as set forth in claim 77, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer and a SiCH layer.

80. A method as set forth in claim 77, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiOCNH layer formed thereon.

81. A method as set forth in claim 77, wherein said barrier insulating layer has a multi-layered structure comprising a SiCNH layer, and a SiCH layer formed thereon.

82. A method as set forth in claim 72, wherein said copper wiring pattern contains at least one anti-migration substance selected from a group consisting of silicon (Si), aluminum (Al), tungsten (W), magnesium (Mg), beryllium (Be), zinc (Zn),

lead (Pb), cadmium (Cd), gold (Au), mercury (Hg), platinum (Pt), zirconium (Zr), titanium (Ti), tin (Sn), nickel (Ni), and iron (Fe).